Massachusetts Institute of Technology
School of Engineering Faculty Personnel Record

Date: April 21, 2004

Full Name: Charles E. Leiserson
Department: Electrical Engineering and Computer Science

1. Date of Birth:

November 10, 1953

2. Citizenship:

U.S.A.

3. Education:

School	Degree	Date
Yale University	B. S. (*cum laude*)	May 1975
Carnegie Mellon University	Ph.D.	Dec. 1981

4. Title of Thesis for Most Advanced Degree:

Area-Efficient VLSI Computation

5. Principal Fields of Interest:

Analysis of algorithms
Parallel algorithms and architectures
Digital hardware and computing machinery
Supercomputing technologies
Computer network architecture
Parallel languages and runtime systems
Parallel and distributed computing
Scalable computing systems
Distance education and interaction
Computer chess

6. Name and Rank of Other Department Faculty in the Same Field:

Anant Agarwal, Professor
Saman Amarasinghe, Associate Professor
Krste Asanovic, Associate Professor
Arvind, Professor
Jack Dennis, Professor Emeritus
Eric Demaine, Assistant Professor
Shafi Goldwasser, Professor
Piotr Indyk, Assistant Professor

David Karger, Associate Professor
Nancy A. Lynch, Professor
Albert R. Meyer, Professor
Silvio Micali, Professor
Martin Rinard, Associate Professor
Ronald L. Rivest, Professor
Madhu Sudan, Professor

7. Name and Rank of Faculty in Other Departments in the Same Field:

Alan Edelman, Professor (Mathemeatics)
Bonnie Berger, Professor (Mathematics)
Michel Goemans, Professor (Mathematics)
F. Thomson Leighton, Professor (Mathematics)
Michael F. Sipser, Professor (Mathematics)
Daniel Spielman, Associate Professor (Mathematics)

8. Non-MIT Experience:

Employer	**Position**	**Beginning**	**Ending**
International Computing Centre (*United Nations, Geneva, Switzerland*)	Programmer Assistant	June 1973	Sept. 1973
Yale University (*Department of Computer Science*)	Programmer	May 1974	Sept. 1974
POS Corporation (*New Haven, CT*)	Software Consultant (*part time*)	Sept. 1974	May 1975
Computervision Corporation (*Bedford, MA*)	Programmer	June 1975	Sept. 1976
Max Planck Institute für Informatik (*Saarbrücken, Germany*)	Fachbeirat (Visiting Committee)	Sept. 1992	present
Ecole Normale Superieure de Lyon (*Lyon, France*)	Visiting Professor	June 1993	July 1993
National University of Singapore (*Republic of Singapore*)	Shaw Visiting Professor	August 1995	August 1996
Akamai Technologies	Director of System	June 1999	

(*Cambridge, MA*)	Architecture

9. History of MIT Appointments:

Rank	**Beginning**	**Ending**
Assistant Professor	Jan. 1981	June 1984
Associate Professor	July 1984	June 1988
Associate Professor (with tenure)	July 1988	June 1992
Professor	July 1992	present

10. Consulting Record:

Firm	**Beginning**	**Ending**
MIT Lincoln Laboratory	Feb. 1982	Aug. 1984
AT&T Bell Laboratories	Jan. 1983	Dec. 1986
Harris Corporation (GASD)	Feb. 1983	May 1985
Cognition	Dec. 1984	June 1985
Analog Devices	Feb. 1985	June 1985
Thinking Machines	July 1985	Aug. 1994
Harris Corporation (GCSD)	May 1986	June 1986
W. W. Oliver Company	January 1987	Jan. 1987
Wolfsort Corporation	March 1991	Mar. 1991
National University of Singapore, Adjunct Professor	Sept. 1996	present
NKK Corporation	Mar. 1997	Mar. 1997
Pratt & Whitney	May 1997	Dec. 1999
EMC^2 Corporation	June 1998	Feb. 1999
Akamai Technologies	June 1999	present
Etisalat University, UAE	April 2003	present
Real Networks	May 2003	present

11. Department and Institute Committees, Other Assigned Duties:

Activity	**Beginning**	**Ending**
Graduate Counselor (EECS)	Sept. 1981	May 1988
Area II Committee (EECS)	Sept. 1981	May 1988
LCS Executive Committee	Sept. 1981	Sept. 1982
Graduate Admissions Committee (EECS)	Nov. 1981	May 1985
LCS Executive Committee	Sept. 1984	Dec. 1987
MIT/LCS Student Workshop (Chairman)	July 1990	July 1994
Undergraduate Advisor (EECS)	Sept. 1990	May 1995
VI-A liaison for IBM Research	Feb. 1991	Mar. 1993
MIT VLSI &Parallel Systems Student Workshop (Chairman)	May 1991	July 1991
MIT VLSI & Parallel Systems Student Workshop (Chairman)	May 1992	July 1992
Leader, Supercomputing Technologies Group	Sept. 1993	present
MIT Supercomputing Technologies Student Workshop (Chairman)	May 1993	July 1993
Graduate Counselor (EECS)	Sept. 1996	present

Area II Committee (EECS)	Sept. 1996	present
EECS Professional Education Policy Committee	Mar. 1992	May 1993
MIT Commencement Committee	Sept. 1996	present
Singapore Engineering Education Assessment Committee	Mar. 1997	June 1998
MIT Student Workshop (Chairman)	Apr. 1997	July 1997
EECS Client Building Committee	Apr. 1997	present
EECS Faculty Search Committee	Nov. 1998	Sept. 1999

12. Government Committees, Service, etc.:

Activity	**Date**
NSF *Ad Hoc* Committee on Supercomputing Software	1985
DARPA/ISTO TeraOps Working Group	1987–1989
Joint DARPA/NSF and ESPRIT Exploratory Workshop on Information Science and Technology	1990

13. Awards Received:

Award	**Date**
Benjamin F. Barge Prize in Mathematics (*Yale University*)	1972
Hertz Fellowship	1977
Hertz Doctoral Thesis Award	1982
ACM Doctoral Dissertation Award	1982
NSF Presidential Young Investigator Award	1985
IEEE Int. Conf. on Parallel Processing Best Presentation Award	1985
IEEE Int. Conf. on Parallel Processing Best Presentation Award (with Thomas H. Cormen)	1986
IEEE Int. Conf. on Parallel Processing Most Original Paper Award (with Bruce M. Maggs)	1986
Best 1990 Professional and Scholarly Book in Computer Science and Data Processing, Association of American Publishers (with Thomas H. Cormen and Ronald L. Rivest)	1990
Richard B. Adler Scholar, MIT EECS Department	1991
3rd Place in ACM International Computer Chess Championship for StarTech	1993
3rd Place in ACM International Computer Chess Championship for ⋆Socrates	1994
Recognition of Service Award by ACM for service as Conference General Chair for SPAA'95	1995
2nd Place in ICCA 8th Computer Chess World Championship for ⋆Socrates 2.0	1995
Recognition of Service Award by ACM for service as Conference General Chair for SPAA'96	1996
1st Place in Dutch Open Computer Chess Championship for Cilkchess	1996
IEEE Computer Society Distinguished Visitor for the Asia-Pacific Region	1996–1998
Recognition of Service Award by ACM for service as Conference General Chair for SPAA'97	1997
2nd Place in Dutch Open Computer Chess Championship for Cilkchess	1997
1st Prize in the International Conference on Functional Programming's	1998

ICFP Programming Contest

2nd Place in Dutch Open Computer Chess Championship for Cilkchess	1998

14. Organization Membership:

Organization	**Offices Held**
AAAS	
ACM	
IEEE	
SIAM	
ACM Turing Award Committee	1983–1987, (Chair, 1986)
Journal of VLSI and Computer Systems	Editor, 1983–1985
1982 MIT VLSI Conference	Program Committee
1984 MIT VLSI Conference	Program Committee
1986 MIT VLSI Conference Committee	Program Chair
Springer-Verlag Texts and Monographs in Computer Science	Editorial Board, 1986–1993
1986 IEEE Symposium on Foundations of Computer Science	Program Committee
Journal of Parallel and Distributed Computing	Editor, 1986–1988
Applied Mathematics Letters	Editor, 1987–1990
1989 ACM Symposium on Parallel Algorithms and Architectures	Program Committee
1989 IEEE Symposium on Foundations of Computer Science	Program Committee
Supercomputing '91	Program Committee
1993 DIMACS Workshop on Models, Architectures, and Technologies for Parallel Computation	Organizing Committee
1994 ACM Symposium on Parallel Algorithms and Architectures	Program Chair
ACM Symposium on Parallel Algorithms and Architectures	General Chair, 1994–1997
Journal of Computer and Systems Science	Guest Editor, 1996
SC'xy Steering Committee, 1999	
Journal of Parallel and Distributed Computing	Advisory Board, 1999
2003 ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming	Program Committee

15. Patents and Patent Applications Pending:

1. H. T. Kung and Charles E. Leiserson, "Systolic array apparatus for matrix computations," *United States Patent* 494,659, March 29, 1984.

2. Thomas H. Cormen and Charles E. Leiserson, "A message merging device," *United States Patent* 4,922,246, May 1, 1990.

3. Robert C. Zak, Charles E. Leiserson, Bradley C. Kuszmaul, Shaw-Wen Yang, W. Daniel Hillis, David C. Douglas, and David Potter, "Parallel computer system including arrangement for transferring messages from a source processor to selected ones of a plurality of destination processors and combining responses," *United States Patent* 5,265,207, November 23, 1993.

4. Charles E. Leiserson, Robert C. Zak, W. Daniel, Hillis, Bradley C. Kuszmaul, Jeffrey V. Hill, "Parallel computer system including request distribution network for distributing processing requests to selected sets of processors in parallel," *United States Patent* 5,388,214, February 7, 1995.

5. Bradley C. Kuszmaul, Charles E. Leiserson, Shaw-Wen Yang, Carl R. Feynman, W. Daniel Hillis, David Wells, Cynthia J. Spiller, "Parallel computer system including arrangement for quickly draining messages from message router," *United States Patent* 5,390,298, February 14, 1995.

6. Timothy N. Weller and Charles E. Leiserson, "Content delivery network service provider (CDNSP)-managed content delivery network (CDN) for network service provider (NSP)," *United States Patent Application* 10/114,080, filed April 2, 2002.

Teaching Experience of Charles E. Leiserson:

Term	**Subject**	**Title**	**Role**
ST 81	6.001	*Structure and Interpretation of Computer Programs*	Recitation (2 sections)
FT 81	6.032	*Computation Structures*	Recitation (2 sections)
ST 82	6.002	*Circuits and Electronics*	Recitation (2 sections)
FT 82	6.033	*Computer System Engineering*	Recitation (2 sections)
ST 83	6.045	*Computability, Automata, and Formal Languages*	Lectures, in charge
FT 83	6.045	*Computability, Automata, and Formal Languages*	Lectures, in charge
ST 84	6.895	*VLSI Algorithms*	Lectures, in charge
FT 84	6.001	*Structure and Interpretation of Computer Programs*	Recitation (2 sections)
FT 85	6.046	*Introduction to Algorithms*	Lectures, in charge
ST 86	6.891	*Theory of Computing Machinery*	Lectures, in charge
FT 86	6.046	*Introduction to Algorithms*	Lectures, in charge
FT 86	6.848	*Introduction to VLSI and Parallel Computation*	Lectures
ST 87	6.849	*Advanced VLSI and Parallel Computation*	Lectures, in charge
SS 87	6.84s	*Parallel Algorithms and Architectures*	Lectures, in charge
FT 87	6.046	*Introduction to Algorithms*	Lectures, in charge
FT 87	6.848	*Introduction to VLSI and Parallel Computation*	Lectures
SS 88	6.84s	*Parallel Algorithms and Architectures*	Lectures, in charge
ST 89	6.004	*Computation Structures*	Recitation (2 sections)

SS 89	6.84s	*Parallel Algorithms and Architectures*	Lectures, in charge
FT 89	6.046	*Introduction to Algorithms*	Lectures, in charge
SS 90	6.84s	*Parallel Algorithms and Architectures*	Lectures, in charge
FT 90	6.046	*Introduction to Algorithms*	Lectures, in charge
ST 91	6.046	*Introduction to Algorithms*	Lectures, in charge
SS 91	6.84s	*Parallel Algorithms and Architectures*	Lectures, in charge
FT 91		Richard B. Adler Scholar (6.035 and 6.918)	
ST 92	6.851	*Theory of Algorithms*	Lectures, in charge
FT 92	6.004	*Computation Structures*	Recitation (1 section)
ST 93	6.851	*Theory of Algorithms*	Lectures, in charge
SS 93	6.84s	*Parallel Algorithms and Architectures*	Lectures, in charge
FT 93	6.042	*Mathematics for Computer Science*	Development, in charge
ST 94	6.042	*Mathematics for Computer Science*	Lectures, in charge
FT 94	6.042	*Mathematics for Computer Science*	Lectures, in charge
ST 95	6.046	*Introduction to Algorithms*	Lectures, in charge
ST 96	CS413	*Introduction to Parallel Systems* (National University of Singapore)	Lectures, in charge
FT 96	6.046	*Introduction to Algorithms*	Lectures, in charge
ST 97	6.892	*Theory of Parallel Systems*	Lectures, in charge
FT 98	6.972	*The Structure of Engineering Revolutions*	Development, in charge.
ST 98	6.046	*Introduction to Algorithms*	Lectures, in charge
ST 99	6.046	*Introduction to Algorithms*	Lectures, in charge
FT 99	6.046	*Introduction to Algorithms*	Lectures, in charge
FT 01	6.046	*Introduction to Algorithms*	Lectures, in charge
ST 02	6.033	*Computer System Engineering*	Recitation (2 sections)
FT 02	6.042	*Mathematics for Computer Science*	Lectures, development
ST 03	6.042	*Mathematics for Computer Science*	Lectures, in charge

Publications of Charles E. Leiserson:

16. Books:

1. Charles E. Leiserson, *Area-Efficient VLSI Computation*, ACM Doctoral Dissertation Award Series, MIT Press, Cambridge, Massachusetts, 1983. (Won the ACM award for best Ph.D. thesis in computer science for the 1981–1982 academic year, as well as the John and Fannie Hertz Foundation award for best Ph.D. thesis in 1981.)

2. Charles E. Leiserson, editor, *Advanced Research in VLSI,* MIT Press, Cambridge, Massachusetts, 1986.

3. Thomas H. Cormen, Charles E. Leiserson, and Ronald L. Rivest, *Introduction to Algorithms*, MIT Press and McGraw-Hill, 1990. Chosen by the Association of American Publishers as the Best 1990 Professional and Scholarly Book in Computer Science and Data Processing. Translated into eight languages.

4. Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, and Clifford Stein, *Introduction to Algorithms*, second edition, MIT Press and McGraw-Hill, 2001.

17. Papers in Refereed Journals:

1. Charles E. Leiserson and James B. Saxe, "Optimizing synchronous systems," *Journal of VLSI and Computer Systems,* Vol. 1, No. 1, Spring 1983, pp. 41–67. An early version appears in the *Twenty-Second Annual Symposium on Foundations of Computer Science,* IEEE Computer Society, November 1981, pp. 23–36.

2. Charles E. Leiserson and Ron Y. Pinter, "Optimal placement for river routing," *SIAM Journal on Computing,* Vol. 12, No. 3, August 1983, pp. 447–462. An early version appears in *CMU Conference on VLSI Systems and Computations,* Pittsburgh, Pennsylvania, October 1981, pp. 126–142.

3. Sandeep N. Bhatt and Charles E. Leiserson, "How to assemble tree machines," *Advances in Computing Research,* Vol. 2, 1984, pp. 95–114. An early version appears in the *Fourteenth Annual ACM Symposium on Theory of Computing,* San Francisco, California, ACM Special Interest Group for Automata and Computability Theory, May 1982, pp. 77–84.

4. Benny Chor, Charles E. Leiserson, Ronald L. Rivest, and James Shearer, "An application of number theory to the organization of raster-graphics memory," *JACM*, Vol. 33, No. 1, January 1986, pp. 86–104. An early version by the first three authors appears in the *Twenty-Third Annual Symposium on Foundations of Computer Science,* Chicago, Illinois, IEEE Computer Society, November 1982, pp. 92–99.

5. Tom Leighton and Charles E. Leiserson, "Wafer-scale integration of systolic arrays," *IEEE Transactions on Computers,* Vol. C-34, No. 5, May 1985, pp. 448–461. An early version appears in the *Twenty-Third Annual Symposium on Foundations of Computer Science,* Chicago, Illinois, IEEE Computer Society, November 1982, pp. 297–311.

6. Charles E. Leiserson, "Fat-trees: universal networks for hardware-efficient supercomputing," *IEEE Transactions on Computers,* Vol. C-34, No. 10, October 1985, pp. 892–901. An early version appears in the *1985 International Conference on Parallel Processing*, St. Charles, Illinois, IEEE Computer Society Press, August 1985, pp. 393–402. (Received Best Presentation Award at the conference.)

7. Ronald I. Greenberg and Charles E. Leiserson, "Randomized routing on fat-trees," *Advances in Computing Research*, Vol. 5, JAI Press, Inc., 1989, pp. 345–374. An early version appears in *Twenty-Sixth Annual Symposium on Foundations of Computer Science*, Portland, Oregon, IEEE Computer Society, October 1985, pp. 241–249.

8. Charles E. Leiserson and James B. Saxe, "A mixed-integer linear programming problem which is efficiently solvable," *Journal of Algorithms,* Vol. 9, 1988, pp. 114–128. An early version appears in *Twenty-First Annual Allerton Conference on Communication, Control, and Computing*, Department of Electrical Engineering and the Coordinated Science Laboratory of the University of Illinois at Urbana-Champaign, Allerton House, Monticello, Illinois, October 1983, pp. 204–213.

9. Charles E. Leiserson and Bruce M. Maggs, "Communication-efficient parallel algorithms for distributed random-access machines," *Algorithmica*, Vol. 3, 1988, pp. 53–77. An early version appears as "Communication-efficient parallel graph algorithms," in *1986 International Conference on Parallel Processing,* St. Charles, Illinois, August 1986, 861–868. (Received Most Original Paper Award at the conference.)

10. Ronald I. Greenberg and Charles E. Leiserson, "A compact layout for the three-dimensional tree of meshes," *Applied Mathematics Letters,* Vol. 1, No. 2, 1988, pp. 171–176.

11. Joe Kilian, Shlomo Kipnis, and Charles E. Leiserson, "The organization of permutation architectures with bussed interconnections," *IEEE Transactions on Computers*, Vol. 39, No. 11, November 1990, pp. 1346–1358. An early version appears in *Twenty-Eighth Annual Symposium on Foundations of Computer Science,* Syracuse, New York, IEEE Computer Society, October 1987, pp. 305–315.

12. Thomas H. Cormen and Charles E. Leiserson, "A hyperconcentrator switch for routing bit-serial messages," *Journal of Parallel and Distributed Computing*, Vol. 10, 1990, pp. 193–204. An early version appears in *1986 International Conference on Parallel Processing,* St. Charles, Illinois, August 1986, pp. 721–728. (Received Best Presentation Award at the conference.)

13. Charles E. Leiserson and James B. Saxe, "Retiming synchronous circuitry," *Algorithmica*, Vol. 6, 1991, pp. 5–35.

14. Charles E. Leiserson, Zahi S. Abuhamdeh, David C. Douglas, Carl R. Feynman, Mahesh N. Ganmukhi, Jeffrey V. Hill, W. Daniel Hillis, Bradley C. Kuszmaul, Margaret A. St. Pierre, David S. Wells, Monica C. Wong, Shaw-Wen Yang, and Robert Zak, "The Network Architecture of the Connection Machine CM-5," *Journal of Parallel and Distributed Computing*, Vol. 33, No. 2, March 15, 1996, pp. 145–158. An early version appears in the *4th Annual ACM Symposium on Parallel Algorithms and Architectures*, San Diego, California, July 1992, pp. 272–285.

15. Robert D. Blumofe and Charles E. Leiserson, "Space-efficient scheduling of multithreaded computations," *SIAM Journal on Computing*, Vol. 7, No. 1, February 1998, pp. 202–229. An early version appears in *Proceedings of the 25th Symposium on Theory of Computing*, ACM, San Diego, California, May, 1993, pp. 362–371.

16. Robert D. Blumofe and Charles E. Leiserson, "Scheduling multithreaded computations by work stealing," *Journal of the ACM*, Vol. 46, No. 5, September 1999, pp. 720–748. An early version appears in the *Thirty-Fifth Annual Symposium on Foundations of Computer Science*, IEEE Computer Society, November 1994, pp. 356–368.

17. Robert D. Blumofe, Christopher F. Joerg, Bradley C. Kuszmaul, Charles E. Leiserson, Keith H. Randall, and Yuli Zhou, "Cilk: An efficient multithreaded runtime system," *Journal of Parallel and Distributed Computing*, Vol. 37, No. 1, August 1996, pp. 55–69. An early version appears in the *Fifth ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, July 1995, pp. 207–216.

18. Alexander T. Ishii, Charles E. Leiserson, and Marios Papaefthymiou, "Optimizing two-phase, level-clocked circuitry," *Journal of the ACM*, Vol. 44, No. 1, January 1997, pp. 148–199.

An early version appears in the *Brown/MIT Conference on Advanced Research in VLSI and Parallel Systems*, Providence, Rhode Island, March 1992, pp. 245–264.

19. Charles E. Leiserson and Keith H. Randall, "Parallel algorithms for the circuit value update problem," *Theory of Computing Systems*, Vol. 30, 1997, pp. 583–597. An early version appears in the *Seventh Annual ACM Symposium on Parallel Algorithms and Architectures*, July 1995, pp. 13–20.

20. Guy. E. Blelloch, Charles E. Leiserson, Bruce M. Maggs, C. Gregory Plaxton, Stephen J. Smith, and Marco Zagha, "An experimental analysis of parallel sorting algorithms," *Theory of Computing Systems*, Vol. 31, No. 2, 1998, pp. 135–167. An early version appears under the title, "A comparison of sorting algorithms for the Connection Machine CM-2," in the *3rd Annual ACM Symposium on Parallel Algorithms and Architectures*, Hilton Head, South Carolina, July 1991, pp. 3–16.

21. Don Dailey and Charles E. Leiserson, "Using Cilk to write multiprocessor chess programs," *Advances in Computer Games*, H.J. van den Herik and B. Monien, eds., volume 9, University of Maastricht, 2001, pp. 25–52.

Papers in Proceedings of Refereed Conferences:

(*Other than early versions of those above.*)

1. H. T. Kung and Charles E. Leiserson, "Systolic arrays (for VLSI)," *Sparse Matrix Proceedings 1978,* I. S. Duff and G. W. Stewart, ed., Knoxville, Tennessee, Society for Industrial and Applied Mathematics, 1979, pp. 256–282.

2. Charles E. Leiserson, "Systolic priority queues," *Proceedings of the Caltech Conference on Very Large Scale Integration,* Charles L. Seitz, ed., Pasadena, California, January 1979, pp. 199–214.

3. Dan Hoey and Charles E. Leiserson, "A layout for the shuffle-exchange network," *1980 International Conference on Parallel Processing,* August 1980, pp. 329–336.

4. Charles E. Leiserson, "Area-efficient graph layouts (for VLSI)," *Twenty-First Annual Symposium on Foundations of Computer Science,* Syracuse, New York, IEEE Computer Society, October 1980, pp. 270–281.

5. Charles E. Leiserson, Flavio M. Rose, and James B. Saxe, "Optimizing synchronous circuitry by retiming," *Third Caltech Conference on VLSI,* Randal Bryant, ed., Pasadena, California, March 1983, pp. 87–116.

6. Charles E. Leiserson, "Systolic and semisystolic design," *IEEE International Conference on Computer Design/VLSI in Computers (ICCD '83),* Rye, New York, October 1983, pp. 627–632.

7. Kyle A. Gallivan and Charles E. Leiserson, "High-performance architectures for adaptive filtering," *SPIE Conference on Real Time Signal Processing*, Vol. 495, No. 7, San Diego, California, August 1984, pp. 30–38.

8. Charles E. Leiserson and F. Miller Maley, "Algorithms for routing and testing routability of planar VLSI layouts," *Proceedings of the 17th Symposium on Theory of Computing,* ACM, Providence, Rhode Island, May 1985, pp. 69–78.
9. Alexander T. Ishii and Charles E. Leiserson, "A timing analysis of level-clocked circuitry," *Proceedings of the Sixth MIT Conference on Advanced Research in VLSI*, April 1990, pp. 113–130.
10. Charles E. Leiserson, Satish Rao, and Sivan Toledo, "Efficient Out-of-Core Algorithms for Linear Relaxation using Blocking Covers," *Thirty-Fourth Annual Symposium on Foundations of Computer Science,* IEEE Computer Society, November 1993, pp. 704–713.
11. Robert D. Blumofe, Matteo Frigo, Christopher F. Joerg, Charles E. Leiserson, and Keith H. Randall, "Dag-consistent distributed shared memory," *Tenth International Parallel Processing Symposium*, IEEE Computer Society, April 1996, pp. 132–141.
12. Robert D. Blumofe, Matteo Frigo, Christopher F. Joerg, Charles E. Leiserson, and Keith H. Randall, "An analysis of dag-consistent distributed shared-memory algorithms," *Eighth Annual ACM Symposium on Parallel Algorithms and Architectures*, June 1996, pp. 297–308.
13. Charles E. Leiserson, "Programming irregular parallel applications in Cilk," *Solving Irregularly Structured Problems in Parallel: 4th International Symposium, IRREGULAR'97*, Paderborn, Germany, June 1997, Springer-Verlag, pp. 61–71.
14. Mingdong Feng and Charles E. Leiserson, "Efficient detection of determinacy races in Cilk programs," *Ninth Annual ACM Symposium on Parallel Algorithms and Architectures*, June 1997, pp. 1–11.
15. Matteo Frigo, Charles E. Leiserson, and Keith Randall, "The implementation of the Cilk-5 multithreaded language," *1998 ACM SIGPLAN Conference on Programming Language Design and Implementation*, Montreal, Canada, June 1998, pp. 212–223.
16. Guang-Ien Cheng, Mingdong Feng, Charles E. Leiserson, Keith H. Randall, and Andrew F. Stark, "Detecting data races in Cilk programs that use locks," *Tenth ACM Symposium on Parallel Algorithms and Architectures*, June 1998, pp. 298–309.
17. Matteo Frigo, Charles E. Leiserson, Harald Prokop, and Sridhar Ramachandran, "Cache-oblivious algorithms," *40th Annual Symposium on Foundations of Computer Science*, New York, New York, October 17–19, 1999, pp. 285–297.
18. Ching Law and Charles E. Leiserson, "A new competitive analysis of randomized caching," *Eleventh Annual International Symposium on Algorithms And Computation*, December 2000, pp. 35–46.

Other Major Publications:

1. H. T. Kung and Charles E. Leiserson, "Algorithms for VLSI processor arrays," Chapter 8.3 of *Introduction to VLSI Systems* by Carver A. Mead and Lynn A. Conway, Addison-Wesley, 1978.

2. Charles E. Leiserson, Jill P. Mesirov, Lena Nekludova, Stephen M. Omohundro, and John Reif, "Solving sparse linear systems via parallel nested dissection on the Connection Machine," *SIAM 1986 National Meeting*, Boston, Mass., July 1986. Also appears as a Thinking Machines Corporation technical memorandum (unnumbered).

3. Tom Leighton and Charles E. Leiserson, "A survey of algorithms for integrating wafer-scale systolic arrays," in *Wafer-Scale Integration*, G. Saucier and J. Trilhe, eds., North-Holland, 1986, pp. 177–195.

4. Charles E. Leiserson and John G. Lewis, "Orderings for parallel sparse symmetric factorization," Chapter 5 of *Parallel Processing for Scientific Computing*, Garry Rodrigue, ed., SIAM, 1989.

5. Charles E. Leiserson, "VLSI theory and parallel supercomputing," Chapter 2 of *Carnegie Mellon University School of Computer Science 25th Anniversary Symposium*, Richard F. Rashid, ed., Addison-Wesley, 1991, pp. 29–44. An early version appeared in *Decennial Caltech Conference on VLSI*, March 1989, MIT Press, pp. 5–16.

6. Charles E. Leiserson, "Timekeeper," *SIGACT News*, Vol. 23, No. 4, ACM Press, Fall 1992, pp. 81–82.

7. Charles E. Leiserson, "Cilk," in *Encyclopedia of Distributed Computing*, Joseph Urban and Partha Dasgupta, editors, Kluwer Academic Publishers, to appear.

8. Charles E. Leiserson and Aske Plaat, "Programming parallel applications in Cilk," *SIAM News*, Vol. 31, No. 4, May 1998, pp. 6–7.

Internal Memoranda and Progress Reports:

(*Other than early versions of those above.*)

1. Sandeep N. Bhatt and Charles E. Leiserson, "Minimizing the longest edge in a VLSI layout," MIT VLSI Memo No. 82-86, May 1981.

2. Charles E. Leiserson and Cynthia A. Phillips, "A space-efficient algorithm for finding the connected components of rectangles in the plane," MIT Laboratory for Computer Science Technical Memorandum MIT/LCS/TM-323, February 1987.

3. Charles E. Leiserson and Cynthia A. Phillips, "Parallel contraction of planar graphs," MIT Laboratory for Computer Science Technical Memorandum MIT/LCS/TM-343, October 1987.

4. Tom Leighton, Charles E. Leiserson, Bruce Maggs, Serge Plotkin, and Joel Wein, "Theory of Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 1, March 1988.

5. Tom Leighton, Charles E. Leiserson, Bruce Maggs, Serge Plotkin, and Joel Wein, "Advanced Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 2, March 1988.

6. C. E. Leiserson, F. T. Leighton, and S. A. Plotkin, editors, "Connection Machine Projects," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 4, January 1989.

7. Tom Leighton, Charles E. Leiserson, and Eric Schwabe, "Theory of Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 6, March 1989.

8. Tom Leighton and Charles E. Leiserson, "Advanced Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 7, December 1989.

9. Tom Leighton, Charles E. Leiserson, and Dina Kravets, "Theory of Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 8, May 1990.

10. Charles E. Leiserson, editor, "Proceedings of the 1991 MIT Student Workshop on VLSI and Parallel Systems," MIT Laboratory for Computer Science Technical Report MIT/LCS/TR-513, August 1991.

11. Alexander T. Ishii, Charles E. Leiserson, and Marios C. Papaefthymiou, "An algorithm for the tramp steamer problem based on mean-weight cycles," MIT Laboratory for Computer Science Technical Memorandum MIT/LCS/TM-457, November 1991.

12. Charles E. Leiserson, editor, "Proceedings of the 1992 MIT Student Workshop on VLSI and Parallel Systems," MIT Laboratory for Computer Science Technical Report MIT/LCS/TR-546, August 1992.

13. Charles E. Leiserson, editor, "Proceedings of the 1993 MIT Student Workshop on Supercomputing Technologies," MIT Laboratory for Computer Science Technical Report MIT/LCS/TR-575, August 1993.

14. Phillip B. Gibbons, Richard M. Karp, Charles E. Leiserson, Gregory M. Papadopolous, editors, "DIMACS Workshop on Models, Architectures, and Technologies for Parallel Computation," DIMACS Center for Discrete Mathematics and Theoretical Computer Science, Technical Report 93-87, September, 1993.

15. Charles E. Leiserson, editor, "Proceedings of the 1994 MIT Student Workshop on Supercomputing Technologies," MIT Laboratory for Computer Science Technical Report MIT/LCS/TR-622, July 1994.

16. Supercomputing Technologies Group, MIT Laboratory for Computer Science, *Cilk-5.2 (Beta 1) Reference Manual*, unpublished manuscript, available on the World Wide Web at `http://supertech.lcs.mit.edu/cilk`, 1998. Earlier versions of this manual are also available.

17. Charles E. Leiserson, Harald Prokop, and Keith H. Randall, "Using de Bruijn sequences to index a 1 in a computer word," unpublished manuscript, available on the World Wide Web at `http://supertech.lcs.mit.edu/cilk`, 1998.

18. Charles E. Leiserson and Harald Prokop, "A Minicourse on Multithreaded Programming," unpublished manuscript, available on the World Wide Web at `http://supertech.lcs.mit.edu/cilk`, 1999.

Invited Lectures:

Systolic Systems

May 1981	MIT, Cambridge, Massachusetts

Optimizing Synchronous Systems

July 1981	Digital Equipment Corporation, Maynard, Massachusetts
September 1981	Harvard University, Cambridge, Massachusetts
December 1981	MIT Lincoln Laboratory, Lexington, Massachusetts

Optimal Placement for River Routing

December 1981	MIT, Cambridge, Massachusetts

Digital Circuit Optimization

May 1982	MIT, Cambridge, Massachusetts

Optimization of Digital Circuitry by Retiming

October 1982	Duke University, Durham, North Carolina
November 1982	University of Rochester, Rochester, New York
January 1983	Bell Laboratories, Murray Hill, New Jersey
April 1984	Brown University, Providence, Rhode Island

Wafer-Scale Integration of Systolic Arrays

November 1982	Carnegie-Mellon University, Pittsburgh, Pennsylvania
March 1983	University of California at Berkeley, Berkeley, California
July 1983	MIT, Cambridge, Massachusetts

Systolic and Semisystolic Systems

July 1983	MIT, Cambridge, Massachusetts
July 1983	Harris Corporation, Melbourne, Florida

Systolic and Semisystolic Design

August 1983	AT&T Bell Laboratories, Murray Hill, New Jersey
August 1983	Princeton University, Princeton, New Jersey

Fat-Trees: Universal Networks for Hardware-Efficient Supercomputing

June 1984	MIT, Cambridge, Massachusetts
June 1984	AT&T Bell Laboratories, Murray Hill, New Jersey
October 1984	IBM Research, Yorktown Heights, New York
January 1985	Bolt, Baranek, and Newman, Inc., Cambridge, Massachusetts

January 1985	Stanford University, Stanford, California
January 1985	University of California at Berkeley, Berkeley, California
January 1985	Lawrence Livermore National Laboratory, Livermore, California
February 1985	University of Minnesota, Minneapolis, Minnesota
February 1985	University of Toronto, Toronto, Canada
March 1985	Cornell University, Ithaca, New York
April 1985	New York University, New York, New York
April 1985	Thinking Machines Corporation, Cambridge, Massachusetts

The Relevance of VLSI Theory to Parallel Supercomputing

January 1986	Microelectronics and Computer Technology Corporation Workshop on Interconnection Networks, Austin, Texas
May 1986	Mathematical Sciences Research Institute, Berkeley, California
June 1986	SIAM Annual Conference, Boston, Massachusetts
November 1987	Siemens-MIT Conference, Munich, West Germany

Communication-Efficient Parallel Graph Algorithms

October 1986	Graph Theory Day (New York Academy of Sciences), Albany, New York

New Machine Models for Synchronous Parallel Algorithms

December 1987	Institute for Mathematics and Its Applications, University of Minnesota, Minneapolis, Minnesota

Very Large Scale Computing

October 1988	Project MAC 25th Anniversary Symposium, MIT, Cambridge, Massachusetts

VLSI Theory and Parallel Supercomputing

March 1989	Decennial Caltech Conference on VLSI, California Institute of Technology, Pasadena, California
April 1989	Thinking Machines Corporation, Cambridge, Massachusetts
September 1990	CMU School of Computer Science 25th Anniversary Symposium, Carnegie Mellon University, Pittsburgh, Pennsylvania
October 1990	Texas Instruments Corporation, Dallas, Texas
December 1990	NEC Research Institute, Princeton, New Jersey
April 1992	AT&T Bell Laboratories, Holmdel, New Jersey

Highly Reliable Large-Scale Computing

November 1990	MIT VLSI Research Review, Cambridge, Massachusetts

A Comparision of Sorting Algorithms for the Connection Machine CM-2

March 1991	Purdue University, West Lafayette, Indiana
March 1991	Indiana University, Bloomington, Indiana
October 1991	University of Texas, Austin, Texas

November 1991	Yale University, New Haven, Connecticut

Engineering Parallel Algorithms

May 1991	Second Annual Workshop on Parallel Algorithms, New Orleans, Louisiana

The Network Architecture of the Connection Machine CM-5

November 1991	Yale University, New Haven, Connecticut
November 1991	Sandia National Laboratory, Albuquerque, New Mexico
April 1992	Carnegie Mellon University, Pittsburgh, Pennsylvania
April 1992	MIT, Cambridge, Massachusetts
May 1992	University of Washington, Seattle, Washington
June 1992	Dartmouth Institute for Advanced Graduate Studies, Hanover, New Hampshire
September 1992	International Conference on Parallel Processing Ecole Normale Superieure de Lyon, Lyon, France
September 1992	Commisariat a l'Energie Atomique, Saclay, France
September 1992	Thinking Machines Corporation, Cambridge, Massachusetts
September 1992	DARPA Joint Microsystems/Computer Systems/HPC Software PI Meeting Daytona, Florida
October 1992	Symposium on New Directions in Parallel and Concurrent Computing New York, New York
October 1992	IEEE Foundations of Computer Science Conference (informal, invited presentation), Pittsburgh, Pennsylvania
November 1992	International Heinz Nixdorf Symposium on Parallel Architectures and Their Efficient Use, Paderborn, Germany
December 1992	IEEE Symposium on Parallel and Distributed Processing (keynote) Dallas, Texas
December 1992	Princeton University, Princeton, New Jersey
December 1992	University of Massachusetts, Amherst, Massachusetts
February 1993	Stanford University, Stanford, California
July 1993	International Workshop on Interconnection Networks, Marseille, France
September 1993	University of Zurich, Zurich, Switzerland
September 1993	Max Planck Institut für Informatik, Saarbrücken, Germany

A Menagerie of Parallel Computing Networks

June 1991	MIT Technology Day, Cambridge, Massachusetts

Special-Purpose vs. General-Purpose Parallel Computing Networks

August 1992	International Conference on Application-Specific Array Processors San Francisco, California (keynote)

How to Interconnect One Million Processors (panel session)

October 1992	Frontiers of Massively Parallel Computation, McLean, Virginia

Space-Efficient Scheduling of Multithreaded Computations

September 1993	DIMACS Workshop on Models, Architectures, and Technologies for Parallel Computation, Rutgers University, New Jersey
December 1993	Universite de Paris-Sud, Paris, France
April 1994	Columbia University Theory Day, New York, New York
September 1994	Carleton University, Ottawa, Canada

Efficient Scheduling of Multithreaded Computations

March 1995	National University of Singapore, Singapore
April 1995	Distinguished Lecture, Carnegie Mellon University, Pittsburgh, Pennsylvania
April 1995	Harvard University, Cambridge, Massachusetts
September 1995	Workshop on High-Performance Computing Activities in Singapore National Supercomputing Research Centre, Singapore

What Is Theoretical Computer Science?

March 1996	Keynote Address, Science Research Seminar, National University of Singapore

Can Multithreaded Programming Save Massively Parallel Computing?

April 1996	Keynote Address, International Parallel Processing Symposium, Honolulu, Hawaii
May 1996	GINTIC Institute of Manufacturing Technology, Singapore

Algorithmic Multithreaded Computing

June 1996	Keynote Address, International Conference on Algorithms and Architectures for Parallel Processing, Singapore
September 1996	Distinguished Lecture, Courant Institute, NYU, New York, New York
November 1996	Theory of Computation Seminar, MIT, Cambridge, MA
November 1996	Distinguished Lecture, University of Maryland, College Park, MD

Efficient Detection of Determinacy Races in Cilk Programs

January 1997	National University of Singapore, Singapore
January 1997	Dartmouth College, Hanover, New Hampshire
June 1997	Max Planck Institut für Informatik, Saarbrücken, Germany
November 1997	Distinguished Lecture, University of California, Santa Barbara
January 1998	DEC Systems Research Center, Palo Alto, CA

Teaching Parallel Algorithms using the Cilk Multithreaded Programming Language

June 1997	Forum on Parallel Computing Curricula, Newport, RI
June 1998	Yale Workshop on Multithreaded Algorithms, New Haven, CT
July 1998	National University of Singapore, Singapore
July 1998	Academia Sinica, Taipei, Taiwan

Algorithmic Multithreaded Programing Using Cilk

July 1997	National University of Singapore, Singapore
January 1998	NASA Ames Research Center, Moffett Field, CA
January 1998	Silicon Graphics, Inc., Mountain View, CA

January 1998	Sun Microsystems, Inc., Palo Alto, CA
August 1998	11th International Workshop on Languages and Compilers for Parallel Computing, Chapel Hill, NC

Programming Shared-Memory Multiprocessors Using the Cilk Multithreaded Language

September 1998	MIT EECS Department Colloquium, Cambridge, MA
September 1998	Intel Corporation, Beaverton, OR
September 1998	University of California, Berkeley; Berkeley, CA
October 1998	Stanford University, Stanford, CA
October 1998	University of Delaware, Wilmington, DL
November 1998	Rice University, Houston, TX
December 1998	5th Intl. Conference on High-Performance Computing, Chennai, India
January 1999	Workshop on Parallel Computing for Irregular Applications, Orlando Florida
March 1999	NTT Corporation, Atsugi, Japan
April 1999	Seminar on High-Level Parallel Programming, Dagstuhl, Germany
May 1999	Understanding the New World of Information '99, Taipei, Taiwan
March 2003	George Washington University, Washington, D.C.

Debugging Multithreaded Programs

September 1998	Microsoft Research, Redmond, WA
November 1998	University of Texas at Austin, Austin, TX

Design and Analysis of Algorithms for Shared-Memory Multiprocessors

May 1999	Workshop on Parallel Algorithms, Atlanta, GA
August 1999	Workshop on Algorithms and Data Structures, Vancouver, CA

Using Cilk to Write Multiprocessor Chess Programs

June 1999	International Conference on Computer Chess, Paderborn, Germany

Theses Supervised by Charles E. Leiserson:

Summary

	Total	**Completed**	**In Progress**
S.B.	17	17	0
S.M.	17	17	0
M.Eng.	13	13	0
Engineers	1	1	0
Doctoral			
As Supervisor:	20	20	0
As Reader:	20	20	0

S.B. Theses and Advanced Undergraduate Projects:

1. David H. Covert, *Graphic Objects That Draw Themselves,* May 1983.

2. Csaba Peter Gabor, *A Comparison of VLSI Designs for Complex Multiplication,* January 1984.

3. David J. Jilk, *Methodology for User-Aided Silicon Compilation,* January 1985.

4. Alexander T. Ishii, *A Comparison of Routing Algorithms for Fat-Tree Supercomputers,* May 1985.

5. Bruce M. Maggs, *Computing Minimum Spanning Trees on a Fat-Tree Architecture,* May 1985.

6. Marie J. Sullivan, *Parallel Graph Algorithms on the Connection Machine,* February 1987.

7. Vu Le Phan, *Massively Parallel Solutions to the Sparse Assignment Problem*, May 1991.

8. Michele L. Monclova, *An Experimental Comparison of Red-Black Trees and Skip Lists*, May 1991.

9. David B. Wilson, *Embedding Weak Hypercubes in Strong Hypercubes*, May 1991. (Winner of the William Martin Prize for best undergraduate computer science thesis at MIT.)

10. Keith Randall, *TIM: A CAD Tool for Designing Two-Phase Level-Clocked Circuitry*, May 1993.

11. Daniel Schmidt, *An Empirical Comparison of Four Heap Data Structures*, August 1994.

12. Tzu-Yi Chen, *Efficient Implementation of Out-of-Core Conjugate Gradient Algorithms*, May 1995. (Honorable Mention in the Computer Research Association's Outstanding Undergraduates Competition.)

13. Arup R. Guha, *Implementation of Band Cholesky Factorization in Cilk*, May 1997.

14. Runako Godfrey, , January 1998.

15. Adrian Soviani, 5×5 *Magic Squares in Cilk*, May 1999.

16. Svetoslav Tzvetkov, *Parallel Memory Allocation*, May 1999.

17. David Venturini, *Chess Endgame Database Compression*, May 1999.

S.M. Theses:

1. Martin I. Eiger, *Analysis of Algorithms to Compute Wirings Within Test Fixtures,* June 1985.

2. Cynthia A. Phillips, *Space-Efficient Algorithms for Computational Geometry,* August 1985.

3. F. Miller Maley, *Compaction with Automatic Jog Introduction,* May 1986.

4. Thomas H. Cormen, *Concentrator Switches for Routing Messages in Parallel Computers,* August 1986.

5. Bruce M. Maggs, *Communication-Efficient Parallel Graph Algorithms,* August 1986.

6. Alexander T. Ishii, *A Digital Model for Level-Clocked Circuitry*, January 1989.
7. James A. Park, *Notes on Searching in Multidimensional Monotone Arrays*, January 1989.
8. Jeffrey A. Fried, *VLSI Processor Design for Communication Networks*, January 1989.
9. Marios C. Papaefthymiou, *On Retiming Synchronous Circuitry and Mixed-Integer Optimization*, August 1990.
10. Michael Ernst, *Serializing Parallel Programs by Removing Redundant Computation*, August 1992.
11. Daniel Tunkelang, *An Aesthetic Layout Algorithm for Undirected Graphs*, August 1992.
12. Robert D. Blumofe, *Efficient Storage Management of Multithreaded Computations*, September 1992.
13. Keith Randall, *Virtual Networks: Implementation and Analysis*, May 1993.
14. Matteo Frigo, *The Weakest Reasonable Memory Model*, January 1998.
15. Bin Song, *Scheduling Adaptively Parallel Jobs*, January 1998.
16. Harald Prokop, *Cache-Oblivious Algorithms*, May 1999.
17. Sridhar Ramachandran, *An Algorithmic Theory of Caching*, February 2000.

M.Eng. Theses:

1. Robert C. Miller, *A Type-checking Preprocessor for Cilk 2, a Multithreaded C Language*, May 1995.
2. Howard J. Lu, *Heterogeneous Multithreaded Computing*, May 1995.
3. Daricha Techopitayakul, *Dynamic Parallel Tables*, May 1995.
4. Philip Lisiecki, *Macroscheduling in the Cilk Network of Workstations Environment*, May 1996.
5. Andrew F. Stark, *Debugging Multithreaded Programs that Incorporate User-Level Locking*, May 1998. (Winner of the William Martin Prize for best computer science M.Eng. thesis at MIT.)
6. Guang-Ien Cheng, *Algorithms for Data-Race Detection in Multithreaded Programs*, May 1998.
7. Nathaniel A. Kushman, *Identifying and Fixing Processor Performance Monotonicity Problems: A Case Study of the SUN UltraSPARC*, May 1998.
8. Igor B. Lyubashevskiy, *Portable Fault-Tolerant File I/O*, May 1998.
9. Ching Law, *A New Competitive Analysis of Randomized Caching*, May 1999.
10. Jeremy Sawicki, *Using Cilk for Parallel Computation in MATLAB*, May 1999.

11. David B. Berman, *Efficient Parallel Binary Decision Diagram Construction Using Cilk*, May 2000.

12. Matthew S. DeBergalis, *A Parallel File I/O API for Cilk*, May 2000.

13. Kai Huang, *Data-Race Detection in Transactions-Everywhere Parallel Programming*, May 2003.

Engineers Theses:

1. Flavio Rose, *Models for VLSI Circuits,* March 1982.

Doctoral Theses, Supervisor:

1. Ron Y. Pinter, *Routability and Its Impact on Placement Algorithms for Integrated Circuits,* August 1982. (Cosupervised by Ronald L. Rivest.)

2. Sandeep N. Bhatt, *The Complexity of Graph Layout and Channel Routing for VLSI,* January 1984.

3. Andrew V. Goldberg, *Efficient Graph Algorithms for Sequential and Parallel Computers,* February 1987.

4. F. Miller Maley, *Single-Layer Wire Routing,* August 1987.

5. Serge A. Plotkin, *Graph-Theoretic Techniques for Parallel, Distributed, and Sequential Computation*, August 1988.

6. Guy E. Blelloch, *Scan Primitives and Parallel Vector Models*, September 1988.

7. Bruce M. Maggs, *Locality in Parallel Computation*, September 1989.

8. Ronald I. Greenberg, *Efficient Interconnection Schemes for VLSI and Parallel Computation*, September 1989.

9. Cynthia A. Phillips, *Theoretical and Experimental Analyses of Parallel Combinatorial Algorithms*, October 1989.

10. Shlomo Kipnis, *Organization of Systems with Bussed Interconnections*, August 1990.

11. James K. Park, *The Monge Array: An Abstraction and Its Applications*, May 1991.

12. Alexander T. Ishii, *Timing Verification of Level-Clocked Circuits*, October 1991.

13. Thomas H. Cormen, *Virtual Memory for Data Parallel Computing*, September 1992.

14. Marios C. Papaefthymiou, *Timing Optimization of VLSI and Parallel Systems*, August 1993.

15. Bradley C. Kuszmaul, *Synchronized MIMD Computation*, May 1994.

16. Sivan Toledo, *Quantitative Performance Modeling of Scientific Computations and Creating Locality in Numerical Algorithms*, May 1995.
17. Robert D. Blumofe, *Executing Multithreaded Programs Efficiently*, September 1995.
18. Christopher F. Joerg, *Cilk: A System for Parallel Multithreaded Computing*, January 1996.
19. Keith H. Randall, *Cilk: Efficient Multithreaded Computing*, May 1998.
20. Matteo Frigo, *Portable High-Performance Programs*, June 1999.

Doctoral Theses, Reader:

1. Aloysius K. Mok, *Fundamental Design Problems of Distributed Systems for the Hard-Real-Time Environment,* May 1983.
2. G. A. Boughton, *Routing Networks for Packet Communication Systems,* August 1984.
3. James B. Saxe, *Generalized Transformations on Algorithms: Two Case Studies,* August 1985 (Department of Computer Science, Carnegie-Mellon University).
4. Peter W. Shor, *Random Planar Matching and Bin Packing,* (MIT Mathematics Department), August 1985.
5. Thang Nguyen Bui, *Graph Bisection Algorithms,* January 1986.
6. Daniel Weise, *Hierarchical, Multilevel Verification of MOS/VLSI Circuits,* August 1986.
7. Alan T. Sherman, *Cryptology and VLSI,* October 1986.
8. Mark R. Newman, *Randomness and Robustness in Hypercube Computation*, September 1989.
9. Bonnie Berger, *Using Randomness to Design Efficient Deterministic Algorithms*, May 1990.
10. Eric Schwabe, *Theoretical Issues in Parallel Computation: Hypercube-Related Architectures and Dynamic Structures*, May 1991.
11. Joel Wein, *Parallel Computation and Combinatorial Optimization: Scheduling Algorithms for Parallel Machines and Parallel Algorithms for the Assignment Problem*, August 1991.
12. Filip Van Aelten, *Automatic Procedures for the Behaviorial Verification of Digital Designs*, May 1991.
13. Clifford Stein, *Approximation Algorithms for Multicommodity Flow and Shop Scheduling*, August 1992.
14. David Williamson, *On the Design of Approximation Algorithms for a Class of Graph Problems*, September 1993.
15. Yuan Ma, *Fault-Tolerant Sorting Networks*, June 1994.

16. Feng Ming Dong, *Compilation and Run-Time Environment of Parallel Lisp on Distributed Systems*, May 1995 (Department of Information Systems and Computer Science, National University of Singapore).

17. James Alexander Stuart Fiske, *Thread Scheduling Mechanisms for Multiple-Context Parallel Processors*, May 1995.

18. Parry Husbands, *Interactive Supercomputing*, January 1999.

19. Rajeev Barua, *Maps: A Compiler-Managed Memory System for Software-Exposed Architectures*, January 2000.

20. Russell Schwartz, *The Local Rules Dynamics Model for Self-Assembly Simulation*, February 2000.