

6.896

4.7.2004

LIS.1

BRADLEY C Kuszmaul

"VLSI"

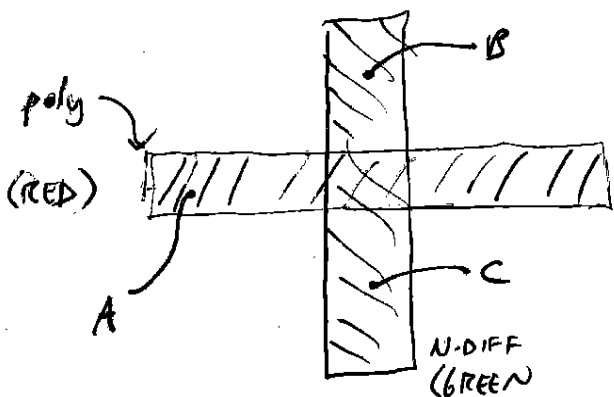
Now we switch gears + talk about the physical design of circuits. Circuits take area on a chip, or volume in a computer. ~~The goal is to analyze circuits,~~ We can analyse circuits for their area just like for their time.

VLSI circuits are drawn with rectangles

Sidebar: Rects Color Code

polysilicon	RED	
N-diffusion	YELLOW	Extra colors in other
P-diff	GREEN	
	<MAGIC>	
	YELLOW (WASTE)	

use MAGIC colors



When you cross green + red you get a transistor.

~~Three regions:~~

- ~~A = all red~~
- ~~B = green on top of red~~
- ~~C = green below red~~

Metal
Oxide
Semiconductor
Field
Effect
Transistor

This is an N-FET because it uses N-diffusion

3 Regions:

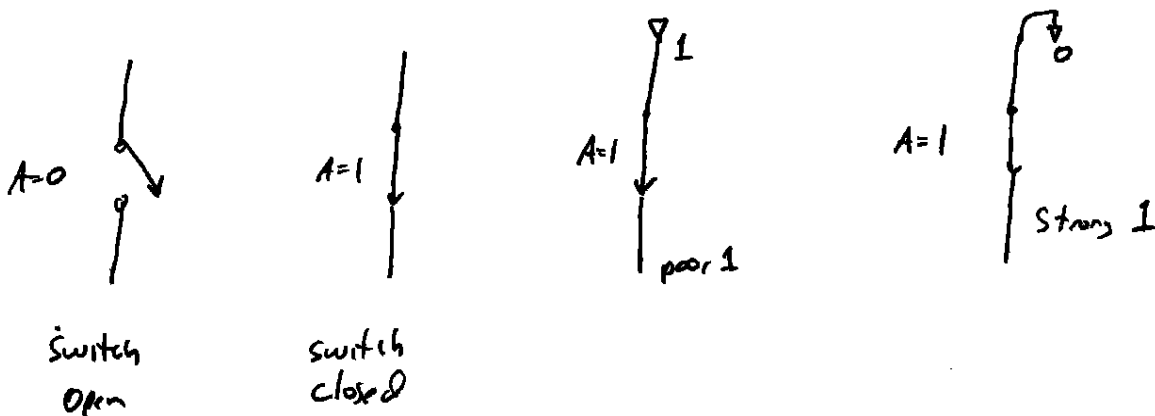
- A - all red area
- B = green ~~area~~ above red
- C = green below red

In schematic this is



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N-FET behavior: (A switch)



But the ~~switch~~ N-FET is only good at transmitting 0's.

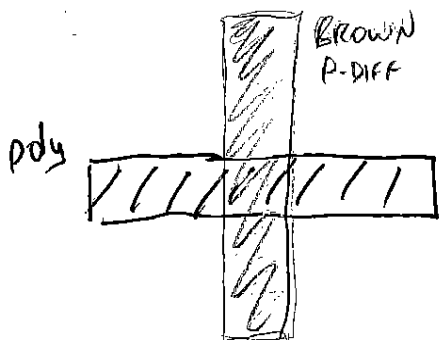
P-FET

could to sidebar:

P-diffusion

BROWN (MAGIC)

GREEN (WASTE)



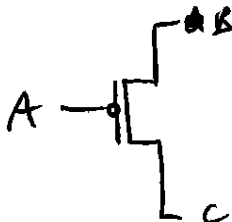
P-FET

Opposite behavior

~~A=1~~ \Rightarrow open

$A=0 \Rightarrow$ closed, passes 1's well

$A=1 \Rightarrow$ open

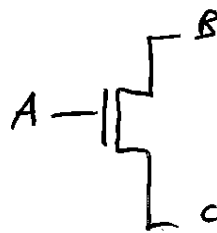


"Bubble means P-FET"
"active low"

N-FET

$A=0$ open

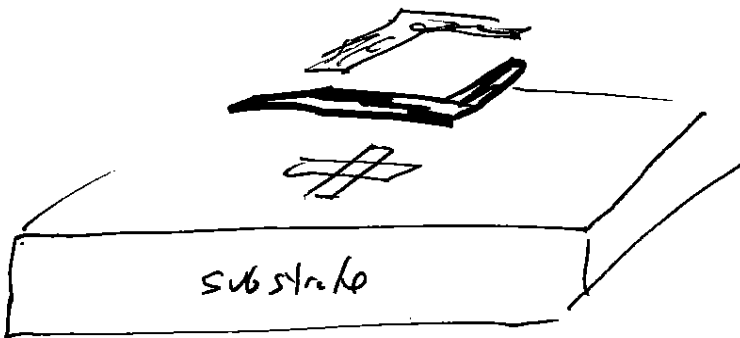
$A=1$ closed, passes 0's well



No bubble = NFET
"active high"

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VLSI is a club sandwich



Bottom layer: substrate

next: diff-scan + poly

next: metal 1 (blue)

next: metal 2 (purple)

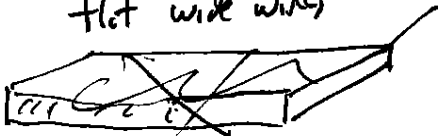
[add to side bar]

[add to sub bar]

Old Days:

1 or 2 layers of metal

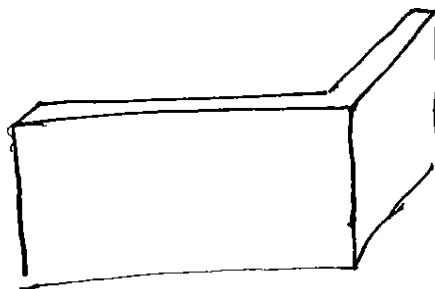
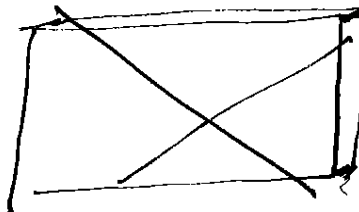
flat wide wires



Now:

20 layers of metal

tall thin wires



(For EE's)

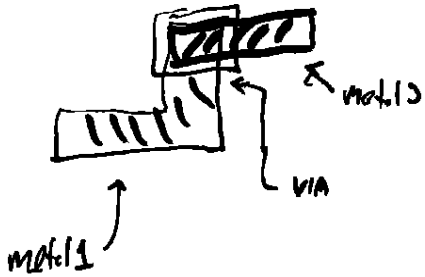
Implications: in old days capacitive coupling mostly between wire + substrate. $C = O(\text{Area of rectangle})$

Now: most ~~cap~~ coupling is between adjacent wires. $C = O(\text{Perimeter of rectangle})$

Lots of crosstalk.

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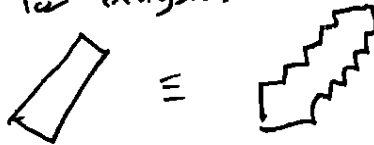
Adjacent layers connected by vias



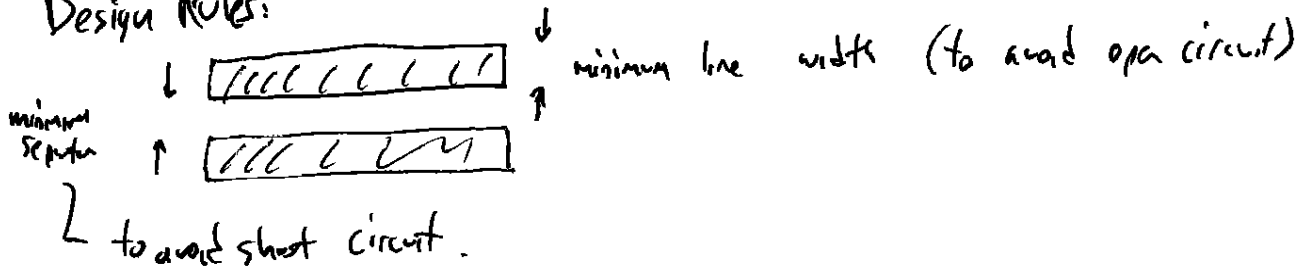
Build a 3-D maze of conductor out of metal.

Angles: Well stuck to 90° angles
Modern technologies include 45° + oth. angles.

ONLY a constant factor for analysis:

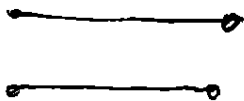


Design Rules:



Can be combined to "center-to-center spacing"

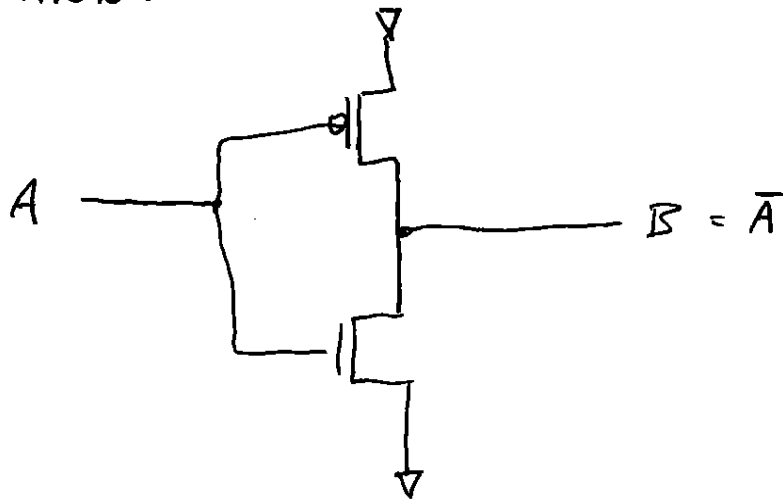
Can draw the lines on a grid, + capture all info.



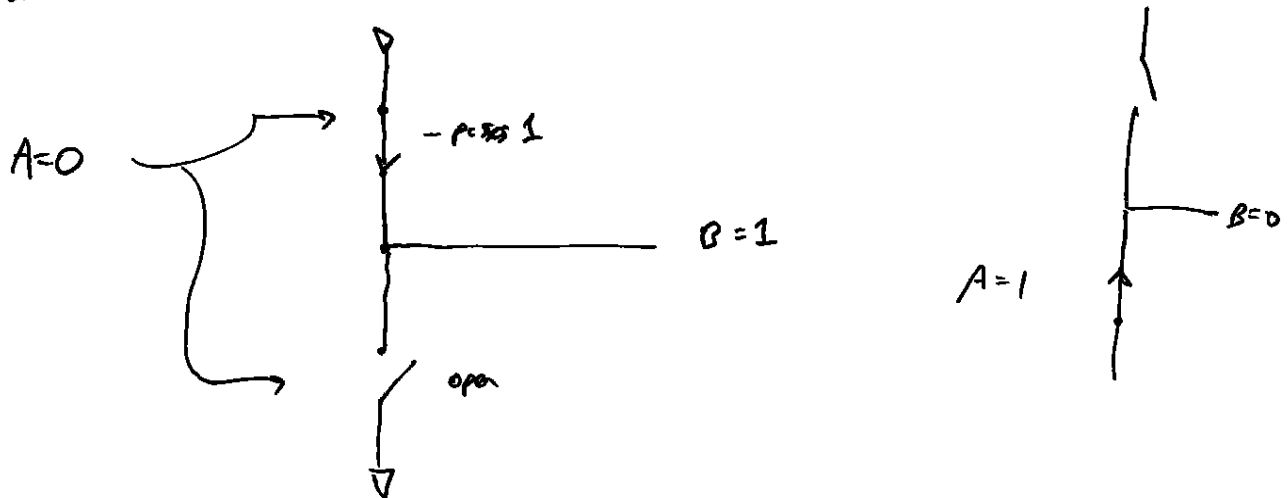
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A CMOS inverter.

Schematic:

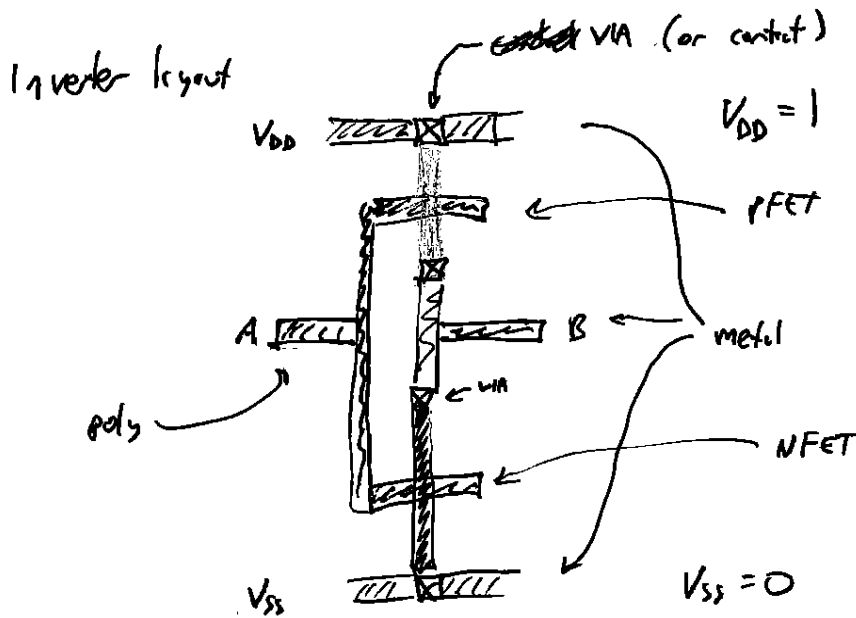


How it works

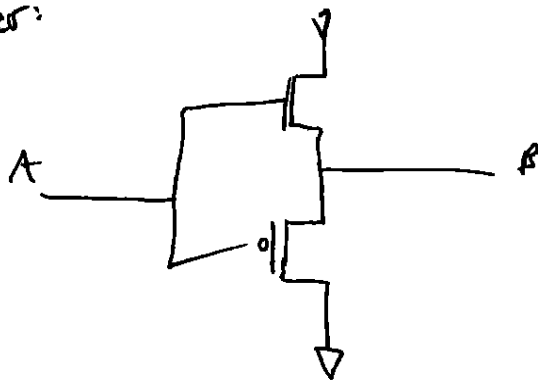


The P-FETS are used to pass 1's, the NFETS to pass 0's.

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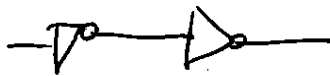
A inverter:



$B = A$

WRONG nFET must be a
good 1

Must use two marks



Q: why would you want an inverter?

A: Transist (long distance, a single takes a power 1 + restore it to a good 1.

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NAND GATE:

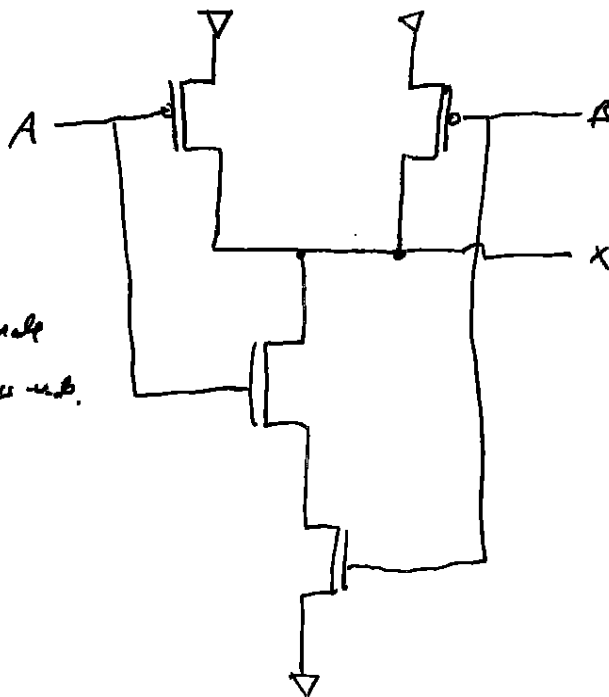
TRUTH TABLE

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

LOGIC SYMBOL

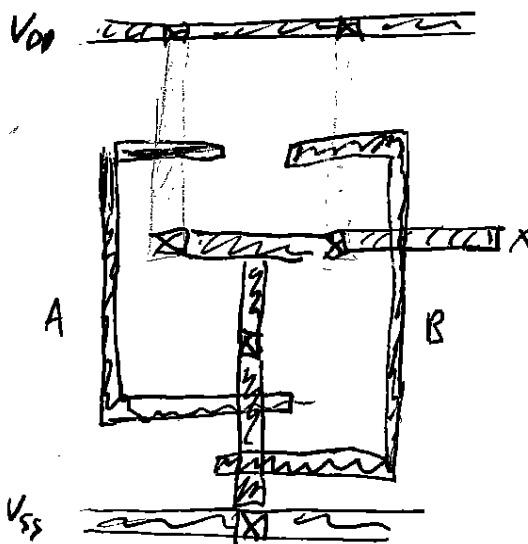


~~TRANSISTOR-CIRCUIT~~
ELECTRONIC SCHEMATIC



If A or B is 0 then output is 1 is made
If A + B are both 1 then output is 0 is made.

LAYOUT



Exercise: ~~Design~~ Design + Draw a 2-input NOR gate

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Side-Trip: DeMorgan's Law

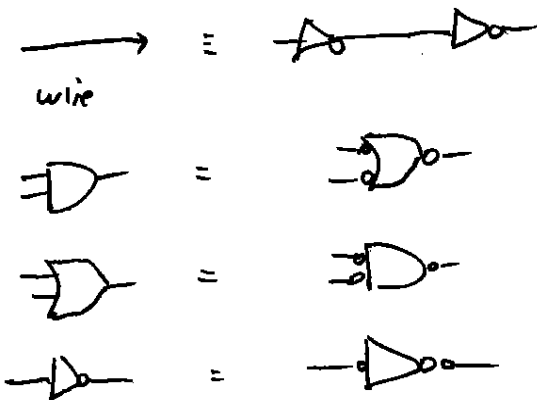
Let A be a circuit comprising inverters, ands, ors, inputs, outputs

Let \bar{A} be the circuit with all ANDs replaced by ORs, & all ORs replaced by ANDs.

Then if we add inverters to the inputs & outputs of \bar{A} we get a functionally equivalent circuit to A [DeMorgan's Law]

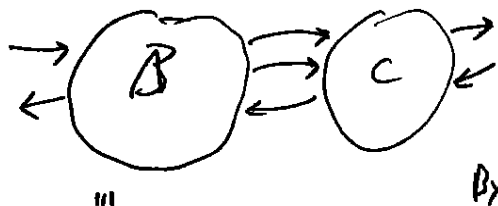
Proof: By induction on circuit size.

Base case

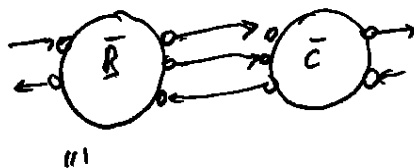


Inductive step:

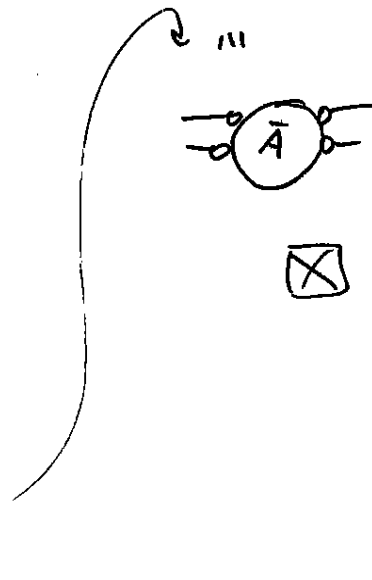
$A =$



By ind. hyp



cancel a

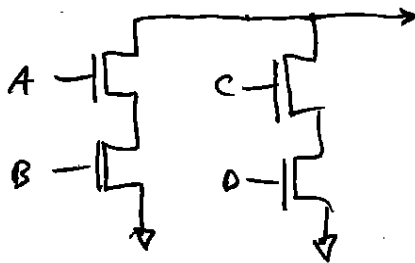


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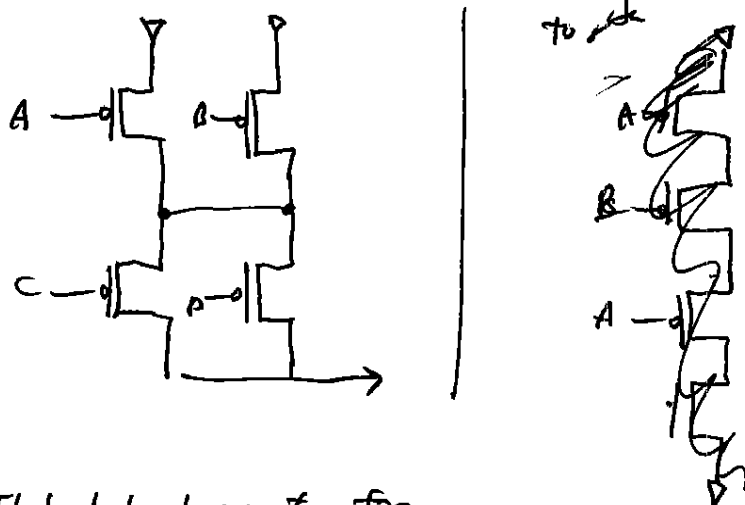
A bigger example: $F = \overline{A \cdot B + C \cdot D}$ Need: a path to 0 iff F is falsea path to 1 iff F is true

The N-side (path to 0)

N-fets create path w/ $\overline{A \cdot B + C \cdot D}$ is false,
i.e. $A \cdot B + C \cdot D$ is trueThe P-side: path to 1 if $\overline{A \cdot B + C \cdot D}$ is true.

Paths made of P-FETs, so all inputs must be inverted to ensure the p-fets switch on. Use DeMorgan

$$\overline{A \cdot B + C \cdot D} \equiv (\overline{A + B}) \cdot (\overline{C + D})$$

Exercise: Design Electrical-Level circuit for
 $F = \overline{(A+B+C) \cdot D}$